AMENDMENTS TO THE CLAIMS

This Listing of Claims will replace all prior versions, and listings, of claims in this application:

Listing of Claims:

1. (Original) A modem for establishing communication between a first device and a second device via a communication medium, said modem for passing a transmit signal generated by the first device via a transmitter to the communication medium and passing a receive signal from the communication medium to a receiver for processing by the first device, said modem coupled to the communication medium through a hybrid circuit, said modem comprising:

a Farrow phase shifter positioned between the first device and the hybrid circuit to shift the phase of the transmit signal;

an equalizer positioned between the hybrid circuit and the first device to minimize intersymbol interference in the receive signal, said equalizer having an adaptive input;

a primary echo sub-canceler having an input coupled between the Farrow phase shifter and the hybrid circuit to receive the phase shifted transmit signal and an output coupled between the hybrid circuit and the equalizer, said primary echo sub-canceler adapted to remove a first portion of an echo in the receive signal;

a post equalizer echo canceler having an input coupled between the Farrow phase shifter and the hybrid circuit to receive the phase shifted transmit signal and an output coupled between said equalizer and the first device, said post equalizer echo canceler adapted to remove a second portion of the echo in the receive signal, said post equalizer echo canceler having an adaptive input; and

a slicer positioned between the output of the post equalizer echo canceler and the first device, said slicer having an output for producing a standard symbol value which is a representation of a current symbol value being supplied at an input of said slicer by the receive signal, the difference between the input and the output of said slicer being supplied to the adaptive input of said equalizer and to the adaptive input of said post equalizer echo canceler.

2. (Original) The modem of claim 1, further comprising:

an interpolator positioned between said Farrow phase shifter and the hybrid circuit to increase the sampling rate representing the phase shifted transmit signal.

3. (Original) The modem of claim 1, wherein said Farrow phase shifter further performs the function of interpolating said transmit signal.

4. (Original) The modem of claim 1, further comprising:

a decimator positioned between the input to the primary echo sub canceler and the hybrid circuit to decrease the sampling rate representing the receive signal.

5. (Original) The modem of claim 4, wherein said equalizer further performs the functions of decimating said receive signal.

6. (Original) The modem of claim 1, further comprising:

a clock having a first clock rate;

at least one divider for reducing said first clock rate to a second clock rate;

a D/A converter coupled between the input of the primary echo sub-canceler and the hybrid circuit for converting the transmit signal from digital to analog, said D/A converter operating at said second clock rate;

an A/D converter coupled between the hybrid circuit and the output of the primary echo sub-canceler for converting the receive signal from analog to digital, said A/D converter operating at said second clock rate;

an add/delete register coupled to said clock for adjusting said first clock rate by at least one clock cycle; and

a phase locked loop having an input coupled between the output of the primary echo sub-canceler and the equalizer and an output coupled to said add/delete register for prompting said add/delete register to adjust said first clock rate by said at least one clock cycle, thereby adjusting said second clock rate.

7. (Original) The modem of claim 1, wherein said post equalizer echo canceler comprises an infinite impulse response filter.

8. (Currently Amended) The modem of claim 1, wherein said primary echo sub-canceler ~~is a 4 sub-canceler echo canceler~~ comprises four sub-cancelers.

9. (Original) A modem for establishing communication between a first device and a second device via a communication medium, said modem for passing an upstream data stream generated by the first device to the communication medium and passing a downstream data stream from the communication medium to the first device, said modem coupled to the communication medium through a hybrid circuit, said modem comprising:

a transmitter having an input for receiving the upstream data stream from the first device and an output for passing a transmit signal;

a Farrow phase shifter having an input coupled to the output of said transmitter and an output, said Farrow phase shifter shifting the phase of said transmit signal;

a D/A converter having a digital input for receiving said phase shifted transmit signal and an analog output for coupling to the hybrid circuit, said D/A converter operating at a first clock rate;

an A/D converter having an analog input for coupling to the hybrid and an digital output, said A/D converter converting a receive signal received from the hybrid circuit from analog to digital, said A/D converter operating at said first clock rate;

a primary echo sub-canceler having an input coupled to the output of said Farrow phase shifter to generate a first echo estimate signal;

a first algebraic combining unit for algebraically subtracting the first echo estimate signal from the receive signal;

an equalizer for processing the receive signal from the first algebraic combining unit to minimize intersymbol interference, said equalizer having an adaptive input;

a post equalizer echo canceler having an input coupled to the output of said Farrow phase shifter, an adaptive input, and an output, said post equalizer echo canceler generating a second echo estimate signal at the output;

a second algebraic combining unit for algebraically subtracting the second echo estimate signal from the receive signal out of said equalizer;

a slicer for receiving the receive signal from said second algebraic combining unit, said slicer having an output for producing a standard symbol value which is a representation of the current symbol value being supplied at an input;

a third algebraic combining unit for algebraically subtracting said current symbol value from said standard symbol value, the difference being supplied to the adaptive input of said equalizer and to the adaptive input of said post equalizer echo canceler; and

a receiver having an input for receiving said standard symbol value and an output for coupling to the first device, said transmitter passing the downstream data stream at the output, the downstream data stream based on said standard symbol values at the output of said slicer.

10. (Original) The modem of claim 9, further comprising a timing adjustment circuit having an input coupled to the output of said first algebraic combining and an output for adjusting said first clock rate.

11. (Original) The modem of claim 10, said timing adjustment circuit comprising at least:

a clock having a second clock rate;

at least one divider for reducing said second clock rate to said first clock rate;

an add/delete register for adjusting said second clock rate by at least one clock cycle; and

a phase locked loop having an input coupled to the output of said first algebraic combining unit and an output coupled to said add/delete register for prompting said add/delete register to adjust said second clock rate by said at least one clock cycle, thereby adjusting said first clock rate.

12. (Original) The modem of claim 9, wherein said equalizer comprises at least a fractionally spaced equalizer.

13. (Original) The modem of claim 12, wherein said equalizer further comprises a decimator.

14. (Original) The modem of claim 9, further comprising:

a decision feedback equalizer having an input coupled to the output of said slicer and an output coupled to an additive input of said second algebraic combining unit.

15. (Original) The modem of claim 9, further comprising:

an interpolator coupled between said Farrow phase shifter and the digital input of said D/A converter; and

a decimator coupled between the output of said first algebraic combining unit and said equalizer.

16. (Original) A sample rate adjustment circuit for adjusting the sampling rate of a CODEC in a modem having a transmit path and a receive path, said circuit comprising:

a clock having a clock rate;

a divider for dividing said clock rate to achieve the sampling rate;

an add/delete register coupled to said clock for adjusting said clock rate by at least on clock cycle based on a signal received at an input;

a primary echo sub-canceler for generating an echo estimate signal based on a transmit signal on the transmit path;

an algebraic combining unit for subtracting said echo estimate signal from a receive signal on the receive path; and

a phase locked loop having an input coupled to an output of said algebraic combining unit and an output coupled to the input of said add/delete register, said phase locked loop controlling said add/delete register to adjust said clock rate by said at least one clock cycle based on the output of said algebraic combining unit, thereby controlling the sampling rate.

17. (Original) A method for use in a modem to establish communication between a first device and a second device via a communication medium, said modem for passing a transmit

signal generated by the first device via a transmitter to the communication medium and passing a receive signal from the communication medium to the first device via a receiver, said modem coupled to the communication medium through a hybrid circuit, said method comprising the steps of:

shifting the phase of the transmit signal using a Farrow structure;

generating a first echo estimate signal from the phase shifted transmit signal using a sub-canceler echo canceler structure;

generating a second echo estimate signal based on the phase shifted transmit signal and an adaptive signal using an infinite impulse response filter;

converting the transmit signal from digital to analog at a sampling rate;

passing the analog transmit signal to the hybrid circuit;

receiving a receive signal from the hybrid circuit;

converting the receive signal from the hybrid circuit from analog to digital at said sampling rate;

subtracting said first echo estimate signal from the receive signal;

adjusting said sampling rate based on the receive signal after subtracting said first echo estimate signal;

equalizing the receive signal based on said adaptive signal;

subtracting said second echo estimate signal from the equalized receive signal;

slicing the equalized receive signal for processing by the first device via the receiver; and

subtracting the receive signal prior to slicing from the downstream data stream after slicing to generate said adaptive signal.

18. (Currently Amended) The method of claim 17, further comprising:

feedback equalizing the equalized receive signal based on the receive ~~dat~~ signal after slicing.

19. (Original) The method of claim 17, wherein said adjusting step comprises the steps of:

generating a clock rate;

dividing said clock rate to achieve said sampling rate;

generating an indicator based on the receive signal after subtracting said first echo estimate signal, said indicator having either a first value or a second value;

subtracting a clock cycle from said clock rate if said indicator is said first value; and

adding a clock cycle to said clock rate if said indicator is said second value.